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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,619	12/04/2003	Shibly S. Ahmed	H1478	5753

45114 7590 03/03/2005

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EXAMINER	
NHU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,619	AHMED ET AL.	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Fried et al (6,583,469 B1), and Yang et al (6,787,854 B1).

Regarding claim 1, Fried, (see figures 1-17, col. 3, lines 35-67, col. 4-6, lines 1-67), teaches a method of manufacturing a semiconductor device, comprising: forming a fin structure12 on an insulator 10u (see figure 14B); forming a gate structure over a portion of the fin structure (see figures 12B); forming a dielectric layer 20 adjacent the gate structure (see figure 15B); removing material 20, 24 in the gate structure (see figures 12A, 14A, 15A); reducing a width of a portion of the fin structure 12 (see figure 14B); depositing a metal 32 to replace the removal material in the gate structure (see figures 16A, 16 B, 17A, 17B).

Regarding claim 1, Yang (see figures 1-8, col. 2, lines 42-67, col. 3-4, lines 1-67), teaches a method of manufacturing a semiconductor device, comprising: forming a fin structure 230 on an insulator 220 (see figure 3); forming a gate structure over a portion of the fin structure (see figures 3); forming a dielectric layer 250 adjacent the gate structure (see figure 3); removing material 410 in the gate structure (see figure 4); reducing a width of a portion of the fin

structure 230 (see figure 4); depositing a metal to replace the removal material in the gate structure (see figures 6-8, col. 6, lines 20-45).

Regarding claim 12, Fried, (see figures 1-18, col. 3, lines 35-67, col. 4-6, lines 1-67, co. 7, lines 1-13), teaches a method of manufacturing a semiconductor device, comprising: forming a fin 12 on an insulator 10u (see figure 14B); forming a gate oxide 16, 30 on sides of the fin (see figures 16B); forming a gate structure over the fin and the gate oxide (see figure 16 B); forming a dielectric layer 20, 24 adjacent the gate structure to define a gate recess (see figure 12 B, 16B); and reducing a width of a portion of the fin 12 below the gate recess (see figures 12B, 16 B); and forming a metal gate 32 in the gate recess (see figures 16B, 17B, 18B).

Regarding claim 18, Fried, (see figures 1-18, col. 3, lines 35-67, col. 4-6, lines 1-67, co. 7, lines 1-13), teaches forming a fin 12 on an insulator 10u (see figure 14B); forming a dielectric cap 18 over the fin (see figure 12B); forming gate oxide layers 16, 30 on opposite sides of the fin (see figure 15B); forming a gate structure over the fin and the dielectric cap (see figures 16A, 16B, 17A, 17B); forming a dielectric layer 20, 24 adjacent the gate structure (see figures 12B, 16B); removing the gate structure to define a gate recess within the dielectric layer 20, 24 and to expose the dielectric cap and gate oxide layers; removing the gate oxide layers from the opposite sides of the fin; reducing a width of the fin 12 below the gate recess (see figures 12B, 14B); forming a metal gate 32 in the gate recess (see figures 16B, 17B, 18B).

Regarding to claims 2-11, 13-17, 19-20, Fried, figures 1-18, col.1-10, and Yang, figures 1-8, col. 1-6, teach depositing a dielectric layer 20, 24 on a silicon layer 10, and etching the dielectric layer and the silicon layer to define the fin structure 12 including a silicon fin and a dielectric cap 18; growing oxide layers 16, 30 on sides of the silicon fin 12; removing the oxide

layers on sides of the silicon fin; depositing a gate material 20, 24 over the fin structure, and selectively etching the gate material to define the gate structure; depositing an oxide material over the gate structure, and polishing (CMP) the oxide material until a top surface of the oxide material is coplanar with a top surface of the gate structure and the top surface of the gate structure is exposed; etching the gate structure to form a gate recess; reducing the width of the portion of the fin structure 12 below the gate recess in a channel region of the semiconductor device.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Yu'890, Fried'090, are cited as of interest.

4. A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned(see 710.02 (b)).

5. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

David Nhu

February 26, 2005